Low Power BS-LFSR Using Single Scan Chain

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Abstract – Power consumption has become a crucial concern in Built In Self Test (BIST) due to the switching activity in the circuit under test(CUT). In this paper we present a novel method which aims at minimizing the total power consumption during testing. This paper presents a low-transition linear feedback shift register (LFSR) that is based on some new observations about the output sequence of a conventional LFSR ,called BS-LFSR. When used to generate test patterns for scan-based built-in self-tests, it reduces the number of transitions that occur at the scan-chain input during scan shift operation by 50% when compared to those patterns produced by a conventional LFSR. Hence, it reduces the overall switching activity in the circuit under test during test applications when compared with existing methods. The BS-LFSR is combined with a scan-chain-ordering algorithm that orders the cells in a way that reduces the average and peak power (scan and capture) in the test cycle or while scanning out a response to a signature analyzer. Experimental results on ISCAS'89 benchmark circuits show up to 65% and 55% reductions in average and peak power, respectively.

Index Terms – Built-in self-test (BIST), linear feedback shift register (LFSR), power consumption, scan-chain ordering, weighted switching activity (WSA).

1. INTRODUCTION

Very Large Scale Integration (VLSI) design plays a significant role in the fabrication of modern Integrated Circuits(ICs) with smaller in size and with more features for any electronics systems. Energy consumption and power dissipation are the major concern in the VLSI design.Low energy consumption has become one of the major design goals in order to prolong battery life. Moreover the amount of energy a circuit consumes is directly reflected in its heat dissipation, however requires expensive packaging and cooling techniques which in turn increases system cost. In addition, as power consumption increases, circuit reliability gets affected adversely due to electro-migration. This is applicable for both Design power and testing power.

A. Prior Work

Several techniques that have been developed to reduce the peak and average power dissipated during scan-based tests. A direct technique to reduce power consumption is by running the test at a slower frequency than that in normal mode. This technique of reducing power consumption, while easy to implement, significantly increases the test application time. Furthermore, it fails in reducing peak-power consumption since it is independent of clock frequency.

Another category of techniques used to reduce the power consumption in scan-based built-in self-tests (BISTs) is by using scan chain-ordering techniques. These techniques aim to reduce the average-power consumption when scanning in test vectors and scanning out captured responses. Although these algorithms aim to reduce average-power consumption, they can reduce the peak power that may occur in the CUT during the scanning cycles, but not the capture power that may result during the test cycle (i.e., between launch and capture).

B. Contribution and Paper Organization

This paper presents a new test pattern generator for low transistions, called the bit-swapping linear feedback shift register (BS-LFSR), that is based on a simple bit-swapping technique applied to the output sequence of a conventional LFSR and designed using a conventional LFSR and a 2 × 1 multiplexer.The proposed BS-LFSR reduces the average and instantaneous weighted switching activity (WSA) during test operation by reducing the number of transitions in the scan input of the CUT. The BSLFSR is combined with a scan-chain-ordering algorithm that reduces the switching activity in both the test cycle (capture power) and the scanning cycles(scanning power).

2. BS-LFSR

The proposed BS-LFSR for test-per-scan BISTs is based upon some new observations concerning the number of transitions produced at the output of an LFSR.

Definition: Two cells in an *n*-bit LFSR are considered to be adjacent if the output of one cell feeds the input of the second directly (i.e., without an intervening XOR gate).

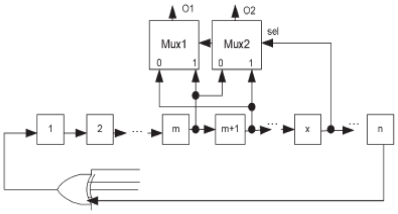

Fig.1. Swapping arrangement for an LFSR

Lemma 1: Each cell in a maximal-length *n*-stage LFSR (internal or external) will produce a number of transitions equal to $2n-1$ after going through a sequence of $2n$ clock cycles.

Proof: The sequence of 1s and 0s that is followed by one bit position of a maximal-length LFSR is commonly referred to as an *m*sequence.Each bit within the LFSR will follow the same *m*-sequence with a one-time-step delay. The *m*-sequence generated by an LFSR of length *n* has a periodicity of $2^{n}-1$. It is a well-known standard property of an *m*-sequence of length *n* that the total number of runs of consecutive occurrences of the same binary digit is 2^{n-1} .The beginning of each run is marked by a transition between 0 and 1;therefore, the total number of transitions for each stage of the LFSR is 2^{n-1}. This lemma can be proved by using the toggle property of the XOR gates used in the feedback of the LFSR

Lemma 2: Consider a maximal-length *n*-stage internal or external LFSR ($n > 2$). We choose one of the cells and swap its value with its adjacent cell if the current value of a third cell in the LFSR is 0 (or 1) and leave the cells unswapped if the third cell has a value of 1 (or 0).Fig. 2 shows this arrangement for an external LFSR (the same is valid for an internal LFSR). In this arrangement, the output of the two cells will have its transition count reduced by *T*saved = $2(n-2)$ transitions.Since the two cells originally produce $2 \times 2n-1$ transitions, then the resulting percentage saving is *T*saved% = 25% . In Lemma 2, the total percentage of transition savings after swapping is 25%. In the case where cell *x* is not directly linked to cell *m* or cell *m*+ 1 through an XOR gate, each of the cells has the same share of savings (i.e., 25%).

Lemmas 3-10 show the special cases where the cell that drives the selection line is linked to one of the swapped cells through an XOR gate. In these configurations, a single cell can save 50% transitions that were originally produced by an LFSR cell. Lemma 3 and its proof are given; other lemmas can be proved in the same way.

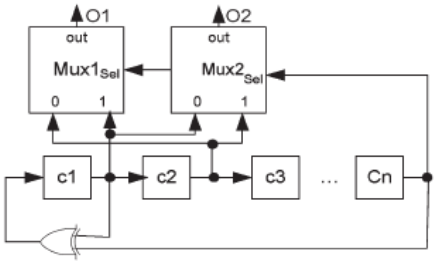

Fig. 2. External LFSR that implements the prime polynomial $x^n + x + 1$ and the proposed swapping arrangement.

Lemma 3: For an external *n*-bit maximal-length LFSR that implements the prime polynomial $x^n + x + 1$ as shown in Fig. 3, if the first two cells (*c*1 and *c*2) have been chosen for swapping and cell *n* as a selection line, then *o*2 (the output of MUX2) will produce a total transition savings of 2^{n-2} compared to the number of transitions produced by each LFSR cell, while *o*1 has no savings (i.e., the savings in transitions is concentrated in one multiplexer output, which means that *o*2 will save 50% of the original transitions produced by each LFSR cell).

Proof: There are eight possible combinations for the initial state of the cells *c*1, *c*2, and *cn*. If we then consider all possible values of the following state, we have two possible combinations (not eight, because the value of *c*2 in the next state is determined by the value of *c*1 in the present state; also, the value of *c*1 in the next state is determined by "*c*1 xor *cn*" in the present state). Table I shows all possible and subsequent states.

TABLE I

POSSIBLE AND SUBSEQUENT STATES FOR CELLS *c*1, *c*2, AND *cn* (see Fig.2)

LFSR outputs of m, m+1								Multiplexers outputs O_1, O_2						
States			Next states			transition			states		Next States		transition	
c_1	c_2	c_n	c_1	c_2	c_n	c_1	c_2	$\sum$	O_1	O_2	O_1	O_2	O_1	O_2	$\sum$
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			0	0	1	0	0	0			0	0	0	0	0
0	0	1	1	0	0	1	0	1	0	0	0	1	0	1	1
			1	0	1	1	0	1			1	0	1	0	1
0	1	0	0	0	0	0	1	1	1	0	0	0	1	0	1
			0	0	1	0	1	1			0	0	1	0	1
0	1	1	1	0	0	1	1	2	0	1	0	1	0	0	0
			1	0	1	1	1	2			1	0	1	1	2
1	0	0	1	1	0	0	1	1	0	1	1	1	1	0	1
			1	1	1	0	1	1			1	1	1	0	1
1	0	1	0	1	0	1	1	2	1	0	1	0	0	0	0
			0	1	1	1	1	2			0	1	1	1	2
1	1	0	1	1	0	0	0	0	1	1	1	1	0	0	0
			1	1	1	0	0	0			1	1	0	0	0
1	1	1	0	1	0	1	0	1	1	1	1	0	0	1	1
			0	1	1	1	0	1			0	1	1	0	1
∑Transitions						8	8	16					8	4	12

It is important to note that the overall savings of 25% is not equally distributed between the outputs of the multiplexers as in Lemma 2.This is because the value of *c*1 in the present state will affect the value of *c*2 and its own value in the next state (*c*2(Next) = *c*1 and *c*1(Next) = "*c*1 xor *cn*"). To see the effect of each cell in transition savings, Table I shows that *o*1 will

save one transition when moving from state (0,0,1) to (1,0,0), from (0,1,1) to (1,0,0), from (1,0,1) to (0,1,0), or from (1,1,1) to (0,1,0). In the same time, $o1$ will increase one transition when moving from (0,1,0) to (0,0,0), from (0,1,0) to (0,0,1),from (1,0,0) to (1,1,0), or from (1,0,0) to (1,1,1). Since $o1$ increases the transitions in four possible scenarios and save transitions in other four scenarios, then it has a neutral overall effect because all the scenarios have the same probabilities.

For $o2$, one transition is saved when moving from (0,1,0) to (0,0,0), from (0,1,0) to (0,0,1), from (0,1,1) to (1,0,0), from (1,0,0) to (1,1,0), from (1,0,0) to (1,1,1), or from (1,0,1) to (0,1,0). At the same time, one additional transition is incurred when moving from state (0,0,1) to (1,0,0) or from (1,1,1) to (0,1,0). This gives $o2$ an overall saving of one transition in four possible scenarios where the initial states has a probability of 1/8 and the final states of probability 1/2;hence, Psave is given by

$$P\text{save} = 1/8 \times 1/2 + 1/8 \times 1/2 + 1/8 \times 1/2 + 1/8 \times 1/2 = 1/4 \quad (1)$$

If the LFSR is allowed to move through a complete cycle of $2n$ states, then Lemma 1 shows that the number of transitions expected to occur in the cell under consideration is 2^{n-1}. Using the swapping approach, in 1/4 of the cases, a saving of one transition will occur,giving a total saving of $1/4 \times 2^n = 2^{n-2}$. Dividing one figure by the other, we see that the total number of transitions saved at $o2$ is 50%.In the special configurations shown in Table II (i.e. Lemmas 3-10), if the cell that saves 50% of the transitions is connected to feed the scan-chain input, then it saves 50% of the transitions inside the scanchain cells, which directly reduces the average power and also the peak power that may result while scanning in a new test vector.Table III shows that there are 104 LFSRs (internal and external) whose sizes lie in the range of 3–168 stages that can be configured to satisfy one or more of the special cases in Table II to concentrate the transition savings in one multiplexer output.

TABLE II

SPECIAL CASES WHERE ONE CELL SAVES 50% OF THE TRANSITIONS

Lemmas	LFSR Polynomial	LFSR Type	Swapped cells		Selection Line	MUX Out 50% Save
			1st	2nd		
Lemma 3	x^n+x+1	External	C_1	C_2	C_n	O_2
Lemma 4	x^n+x+1	Internal	C_1	C_n	C_2	O_2
Lemma 5	$x^n+x^{n-1}+1$	External	C_{n-1}	C_n	C_1	O_1
Lemma 6	$x^n+x^{n-1}+1$	Internal	C_1	C_n	C_{n-1}	O_1
Lemma 7	x^n+x^2+1	External	C_1	C_2	C_n	O_1
Lemma 8	$x^n+x^{n-2}+1$	Internal	C_{n-1}	C_n	C_{n-2}	O_1
Lemma 9	$x^n+x^{n-1}+x^{ym}+\ldots+x^{y2}+x^{y1}+1$	Internal	C_1	C_n	C_{n-1}	O_1
Lemma 10	$x^n+x^{n-2}+x^{ym}+\ldots+x^{y2}+x^{y1}+1$	Internal	C_{n-1}	C_n	C_{n-2}	O_1

TABLE III

LFSRS THAT SATISFY ONE OR MORE OF LEMMAS 3–10

# of LFSR Stages	LFSR settle one or more of Lemmas 3 to 10 in table 2
3-20	3, 4, 5, 6, 7, 8, 11, 12, 13, 14, 15, 16, 19
21-40	21, 22, 24, 26, 27, 29, 30, 32, 34, 35, 37, 38, 40
41-60	42, 43, 44, 45, 46, 48, 50, 51, 53, 54, 56, 59, 60
61-80	61, 62, 63, 64, 66, 67, 69, 70, 74, 75, 76, 77, 78, 80
81-100	83, 85, 86, 88, 90, 91, 92, 93, 96, 99
101-120	101, 102, 104, 107, 109, 110, 112, 114, 115, 116, 117
121-140	122, 123, 125, 126, 127, 128, 131, 133, 136, 138
141-160	141, 143, 144, 146, 147, 149, 152, 153, 154, 155, 156, 157, 158, 160
161-168	162, 163, 164, 165, 166, 168
Total	**104**

3. PROPERTIES OF THE BS-LFSR

There are some important features of the proposed BS-LFSR that make it equivalent to a conventional LFSR. The most important properties of the BS-LFSR are the following.

1) The proposed BS-LFSR generates the same number of 1s and 0s at the output of multiplexers after swapping of two adjacent cells; hence, the probabilities of having a 0 or 1 at a certain cell of the scan chain before applying the test vectors are equal. Hence,the proposed design retains an important feature of any random TPG. Furthermore, the output of the multiplexer depends on three different cells of the LFSR, each of which contains a pseudorandom value. Hence, the expected value at the output can also be considered to be a pseudorandom value.

2) If the BS-LFSR is used to generate test patterns for either test per-clock BIST or for the primary inputs of a scan-based sequential circuit (assuming that they are directly accessible), then consider the case that $c1$ will be swapped with $c2$ and $c3$ with $c4, \ldots, cn-2$ with $cn-1$ according to the value of cn which is connected to the selection line of the multiplexers. In this case, we have the same exhaustive set of test vectors as would be generated by the conventional LFSR, but their order will be different and the overall transitions in the primary inputs of the CUT will be reduced by 25%.

4. SCAN CHAIN REORDERING

In this section,we show how test power can be minimized by appropriately ordering the scan cells of agiven scan chain.The inputs to the proposed procedure are i)a given set of scan flip-flops and ii) a sequence of deterministic test vectors with the corresponding output responses.The output is an ordered scan chain with minimum test power.To tackle this NP-hard problem efficiently,the heuristic procedure operates in two steps: the first one consists in dertermining the chaining of scan cells,the second one consists in identifying the input and output scan cells of the scan chains.

Although the proposed BS-LFSR can achieve good results in reducing the consumption of average power during test and also in minimizing the peak power that may result while scanning a new test vector, it cannot reduce the overall peak power because there are some components that occur while scanning out the captured response or while applying a test vector and capturing a response in the test cycle.To solve these problems, first, the proposed BS-LFSR has been combined with a cell-ordering algorithm that reduces the number of transitions in the scan chain while scanning out the captured response. This will reduce the overall average power and also the peak power that may arise while scanning out a captured response.

In this scan-chain-ordering algorithm, some cells of the ordered scan chain using the algorithm will be reordered again in order to reduce the peak power which may result during the test cycle. This phase mainly depends on an important property of the BS-LFSR.The steps in this algorithm are as follows.

1) Simulate the CUT for the test patterns generated by the BS-LFSR.

2) Identify the group of vectors and responses that violate the peak power.

3) In these vectors, identify the cells that mostly change their values in the test cycle and cause the peak-power violation.

4) For each cell found in step (3), identify the cells that play the key role in the value of this cell in the test cycle.

5) If it is found that, when two cells have a similar value in the applied test vector, the concerned cell will most probably have no transition in the test cycle, then connect these cells together. If it is found that, when two cells have a different value, the cell under consideration will most probably have no transitions in the test cycle, then connect these cells together through an inverter.

TABLE IV

TEST LENGTH NEEDED TO GET TARGET FAULT COVERAGE FOR LFSR AND BS-LFSR

Circuit	n	m	PI	RF%	FC%	Test Length			
						Det.	LFSR	BS-LFSR no order	BS-LFSR with order
S641	32	19	35	0	98.0	53	5120	4910	4970
S838	32	32	35	0	86.5	90	8160	8460	7910
S1196	30	18	14	0	97.0	131	3750	3680	3370
S1238	30	18	14	5.09	91.3	141	3890	3560	3610
S5378	40	179	35	0.88	98.0	244	30110	33700	28900
S9234	40	228	19	6.52	90.0	367	397800	401930	398170
S13207	60	669	31	1.54	95.0	455	49660	47400	48110
S35932	64	1728	35	10.19	89.8	63	18700	16640	16520
S38417	64	1636	28	0.53	96.5	849	118580	125520	117080
S38584	64	1452	12	4.15	94	632	43530	39660	40090

Hence, if no vector violates the peak power, then this phase will not be done. In the worst case, this phase is performed in few subsets of the cells. This is because, if this phase of ordering is done in all cells of the scan chain, then it will destroy the effect of algorithm found in and will substantially increase the computation time.

TABLE V

EXPERIMENTAL RESULTS OF AVERAGE- AND PEAK-POWER REDUCTION OBTAINED BY USING THE PROPOSED TECHNIQUES

Circuit	TL	LFSR			BS-LFSR with cell ordering			%Savings of BS-LFSR	
		FC%	WSA_{avg}	WSA_{pk}	FC%	WSA_{avg}	WSA_{pk}	WSA_{av}	WSA_{pk}
S641	3000	97.84	97.78	153	97.54	42.20	84	57	45
S838	20000	96.15	81.91	151	96.21	33.14	83	60	45
S1196	2000	95.33	53.18	74	95.51	21.52	42	60	43
S1238	3000	91.11	61.20	97	90.97	34.80	59	43	39
S5378	40000	98.42	1143.24	1639	98.40	625.28	993	45	39
S9234	100000	87.27	2817.45	3988	87.28	1108.93	2197	61	45
S13207	100000	96.45	4611.67	7108	96.39	1897.33	4172	59	41
S35932	200	87.88	7945.81	12592	87.89	2793.16	5723	65	55
S38417	100000	95.73	10965.50	16380	95.68	5022.30	10017	54	39
S38584	100000	94.46	11194.65	15974	94.48	5682.72	7851	49	51

5. EXPERIMENTAL RESULTS

A group of experiments was performed on full-scan ISCAS'89 benchmark circuits. In the first set of experiments, the BS-LFSR is evaluated regarding the length of the test sequence needed to achieve a certain fault coverage with and without the scan-chain-ordering algorithm. Table IV shows the results for a set of ten benchmark circuits. The columns labeled *n*, *m*, and PI refer to the sizes of the LFSR, the number of flip-flops in the scan chain, and the number of primary inputs of the CUT, respectively.. The results in Table IV show that the BS-LFSR needs a shorter test length than a conventional LFSR for many circuits even without using the scan chain-ordering algorithm.The second set of experiments is used to evaluate the BS-LFSR together with the proposed scan-chain-ordering algorithm in reducing average and peak power. For each benchmark circuit, the same numbers of conventional LFSR and BS-LFSR patterns are applied to the full scan configuration. Table V shows the obtained results for the same benchmark circuits as in Table IV. The column labeled test length (TL) refers to the number of test vectors applied to the CUT. The next three columns show the FC, average WSA per clock cycle.

Table VI compares the results obtained by the proposed technique with those obtained in [15]. Table VI compares the TL, FC, and average-power reduction (WSAavg) Finally, Table VII compares the results obtained by the proposed technique for peak-power reduction with those obtained in [25]. It is clear from the table that the proposed method has better results for most of the benchmark circuits.

TABLE VI

COMPARISON WITH RESULTS OBTAINED IN [15]

Circuit	Results in [15]			Results of proposed method		
	TL	FC	$\%WSA_{av}$	TL	FC	$\%WSA_{av}$
S641	4096	97.21	38	3000	97.54	57
S838	4096	95.46	50	20000	96.21	60
S1196	4096	95.59	17	2000	95.51	60
S1238	4096	89.41	17	3000	90.97	43
S5378	65536	96.54	43	40000	98.40	45
S9234	524288	90.89	62	100000	87.28	61
S13207	132072	93.66	45	100000	96.39	59
S35932	128	87.84	56	200	87.89	65
S38417	132072	94.99	56	100000	95.68	54
S38584	132072	93.35	59	100000	94.48	49
AVG	**100255**	**93.49**	**44**	**46820**	**94.04**	**55**

TABLE VII

COMPARISON OF PEAK-POWER REDUCTIONS WITH RESULTS IN [25]

Circuit	Results in [25] WSA_{pk} Savings %	Proposed Method WSA_{pk} Savings %
S5378	36.6	39
S9234	38.9	45
S13207	46.1	41
S38417	40.1	39
S38584	35.9	51
AVG	**39.5**	**43.0**

6. CONCLUSION

A low-transition TPG that is based on some observations about transition counts at the output sequence of LFSRs has been presented.The proposed TPG is used to generate test vectors for test-perscan BISTs in order to reduce the switching activity while scanning test vectors into the scan chain. Furthermore, a novel algorithm for scan-chain ordering has been presented. When the BS-LFSR is used together with the proposed scan-chain-ordering algorithm, the average and peak power are substantially reduced. The effect of the proposed design in the fault coverage, test-application time, and hardware area overhead is negligible. Comparisons between proposed design and pervious methods can achieve better results for most tested benchmark circuits.

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